What is claimed is:

1. A pipe latch circuit for storing a plurality of sequentially received first data and second data and outputting them as rising edge output data or falling edge output data, comprising:

a first input register for receiving said first data;

a plurality of first serial pipe latches comprising a plurality of registers connected in series, for selectively storing outputs from said first input register and selectively outputting them;

a first linkage register for storing data outputted from said plurality of first serial pipe latches;

a second input register for receiving said second data;

a plurality of second serial pipe latches comprising a plurality of registers connected in series, for selectively storing outputs from said second input register and selectively outputting them;

a second linkage register for storing data outputted from said plurality of second serial pipe latches;

a multiplexer for selecting data stored in said first register and said second register as rising edge output data or falling edge output data, and outputting them; and

a pipe latch circuit controller for controlling said plurality of first and second serial pipe latches and said multiplexer.

2. The pipe latch circuit as recited in claim 1, wherein said first serial pipe latch includes:

a first path circuit for delivering data outputted from said first input register;

a plurality of registers connected in series, for sequentially delivering data received from said first path circuit;

a plurality of second path circuits provided between said plurality of registers connected in series, for delivering data stored in a register at preceding stage to a register at subsequent stage; and

a third path circuit for delivering data stored in the register at the final stage of said plurality of registers connected in series to said first linkage register.

3. The pipe latch circuit as recited in claim 2, wherein said pipe latch circuit controller includes:

a control signal generator for delivering received clock signals when enabled by data output enable signals, and outputting a plurality of initialization signals as enabled sequentially at each period of said clock signals; and

a plurality of serial pipe latch controllers for receiving said clock signals when enabled by one of said plurality of initialization signals, and sequentially turning on first path circuit through third path circuit provided at said plurality of first serial pipe latches.

4. The pipe latch circuit as recited in claim 3, wherein said serial pipe latch controller includes:

means for counting said clock signals for as many times as total number of first, second and third path circuits provided at said serial pipe latch, when enabled by selected initialization signals; and

a multiplexer for outputting a plurality of input/output control signals that sequentially turn on first, second and third path circuits provided at said serial pipe latch, in response to said counted clock signals.

5. The pipe latch circuit as recited in claim 4, wherein said first and second input registers includes an inverting latch using 2 inverters.

6. A pipe latch circuit as recited in claim 4, wherein said first and second linkage registers includes an inverting latch using 2 inverters.